CSS555(C) Micropower Timer (EEPROM Serial Interface)

Overview

The CSS555 and CSS555C IC's include an internal memory to store configuration and trim data. The data is stored in a non-volatile memory (EEPROM) so that the information is held even when the device is not powered. A four-wire serial interface provides Read/Write access to the EEPROM. To maintain the standard number of 555 pins, four pins have secondary functions. The alternate functions have been defined so they do not interfere with normal timer operation. The EEPROM includes an internal program voltage generator so no external high voltage signals are required to store new data.

The memory access mode is initiated by forcing the CONTROL pin to GND. After the access mode is enabled, the TRIGGER, RESET and OUTPUT pins provide the Serial Clock, Data In and Data Out functions respectively. They are used to enter commands, select an address and input/output data. Each access cycle consists of an eight-bit control byte followed by eight bits of input (or output) data. A detailed description of the pin functions, commands, bit assignments and signal timing is provided in the following figures and tables. A block diagram of the interface circuit is shown below. (see Figure 1)

The EEPROM data can be programmed either before or after the device is installed into the system. If programming is done after installation, a simple interface port can be added to the PCB to allow access to the serial interface pins. Several examples are shown in Figures 7-9.

Block Diagram

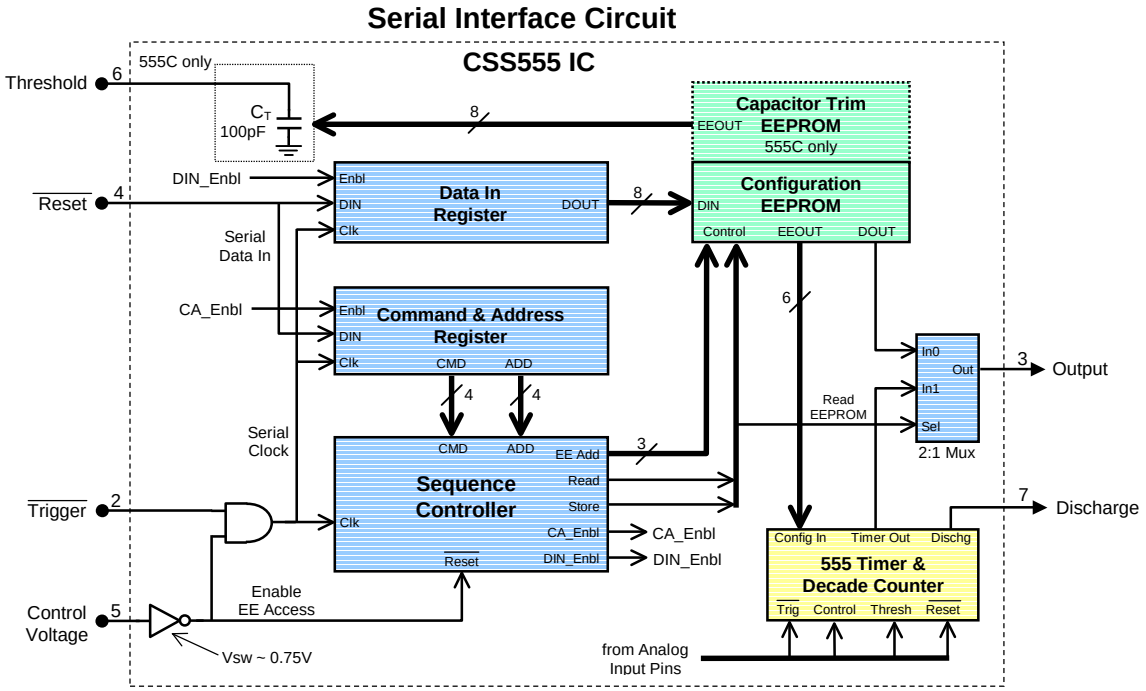

Figure 1

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Serial Interface Description

Four pins have dual functions to provide Read and Write access to the EEPROM. The CONTROL pin is used to enable the EEPROM programming mode. The voltage at the CONTROL pin ($V_{CONTROL}$) is normally set to ⅔V_{DD} by an internal resistive divider. If $V_{CONTROL}$ is held below 0.5V, the programming mode is enabled. When the programming mode is active, three additional pin functions are modified to provide the "Serial Clock", "Serial Data In" and "Serial Data Out" functions. The special pin functions for accessing the EEPROM are listed in Table 1.

Pin Number	Pin Name	Pin Function	
		Primary or Timer Mode	Secondary or EEPROM Program Mode
1	V_{SS}	GND	GND
2	TRIGGER	Start Timer	Serial Clock
3	OUTPUT	Timer Output Pulse	Serial Data Out
4	RESET	Stop Timer	Serial Data In
5	CONTROL	Upper Trip Level (⅔V_{DD})	Program Enable
6	THRESHOLD	Upper Comparator Input	
7	DISCHARGE	C_T Discharge FET	
8	V_{DD}	Positive Supply	Positive Supply

Table 1

In the programming mode, the serial clock is provided by the TRIGGER pin. The RESET pin becomes "Serial Data In" and "Serial Data Out" is provided by the OUTPUT pin. In the normal timing mode, the TRIGGER input is connected to the inverting input of the lower comparator and its switch level is (½ $V_{CONTROL}$). In the programming mode, the TRIGGER input drives a standard CMOS digital input. Its switch level is approximately (½ V_{DD}).

All access cycles start by forcing SCLK low, then the CONTROL pin low and shifting in an eight-bit control byte. (see Figures 2 and 3) The control byte contains a four-bit command and a four-bit address. The command portion is used to specify either a Read or Write cycle. The address portion selects the location to be accessed. A summary of the interface commands is provided in Table 2. If a Read command is entered, the next eight clocks shift the contents of the selected address onto the OUTPUT pin. (Configuration bit assignments are shown in Table 3. Capacitor trim bits (CSS555C only) are entered LSB to MSB.) If a Write command is entered, new data is loaded during the next eight clocks and it is programmed into the EEPROM during the 9th clock pulse. The access cycle is terminated when the CONTROL pin is released. (The internal divider will pull it up to ⅔V_{DD} and the normal timer mode will be re-established.)

Interface Commands (Control Byte)

Mode	Description	Control Pin	Control Byte MSB LSB	
			Address	Command
Normal	555 Timing mode	> 1.0V	xxxx	xxxx
Read EE1	Read Configuration Data	< 0.5V	0001	0001
Read EE2 (Note1)	Read Capacitor Trim Data	< 0.5V	0010	0001
Store EE1	Program Configuration Data	< 0.5V	0001	0010
Store EE2 (Note1)	Program Capacitor Trim Data	< 0.5V	0010	0010

Note1: CSS555C only

Table 2

Configuration Bits (Data Byte)

Counter Configuration MSB LSB	Counter Setting (Multiplier)
xxxxx000	1 (Std. 555)
xxxxx001	10
xxxxx010	100
xxxxx011	1K
xxxxx100	10K
xxxxx101	100K
xxxxx110	1M
xxxxx111	1 (Std. 555)

Mode Control MSB LSB	Function
xxxx0xxx	Astable Mode ("Don't Care" if Std. 555)
xxxx1xxx	Monostable Mode ("Don't Care" if Std. 555)
xxx0xxxx	Micro Power
xxx1xxxx	Low Power
xx0xxxxx	Standard Voltage (Trip levels = ⅓ & ⅔ V_{DD})
xx1xxxxx	Low Voltage (Trip levels = 10% & 90% V_{DD})
Bit 6	Unused
Bit 7	0 if 555, 1 if 555C (Read only)

Table 3

Timing Diagrams

Read EEPROM (1 Byte)

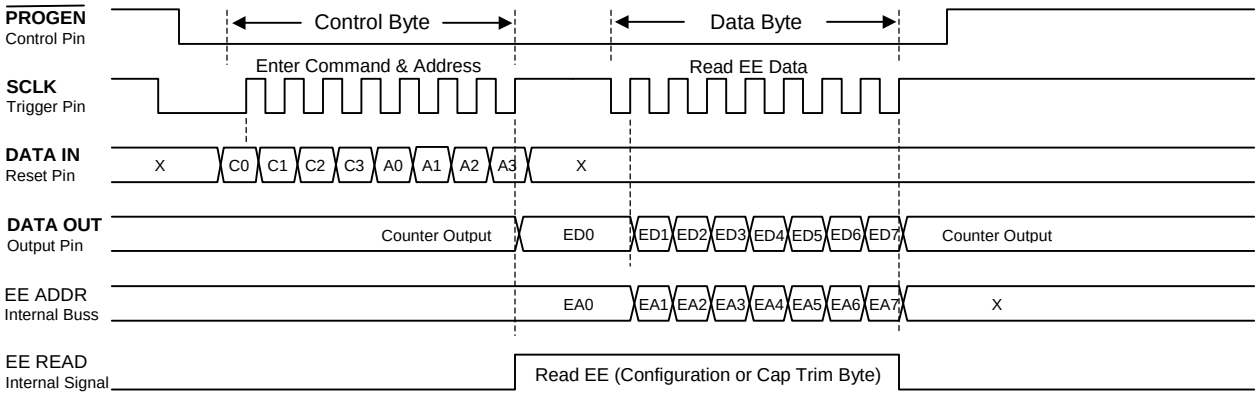

Figure 2

Program EEPROM (1 Byte)

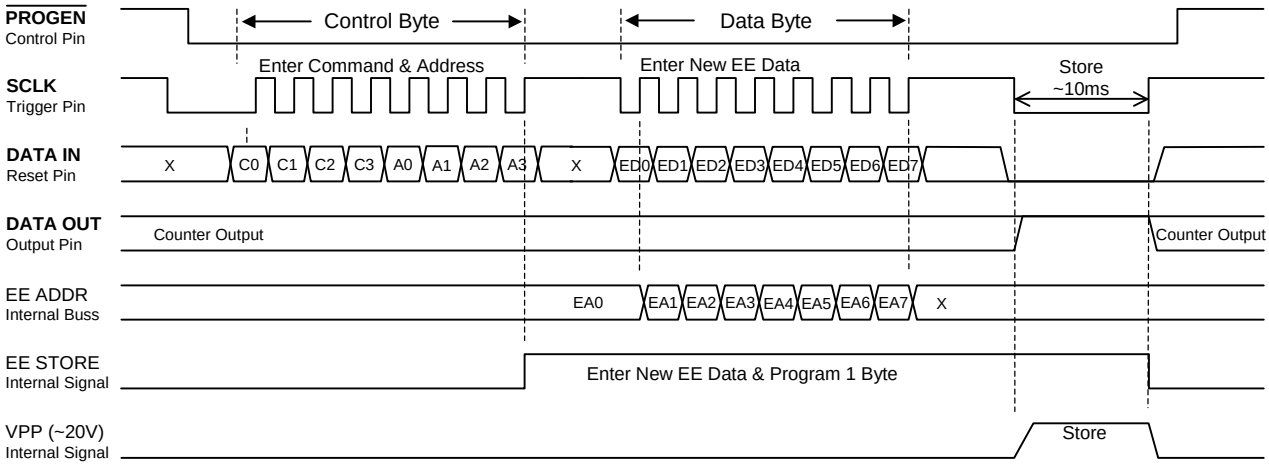

Figure 3

Program Byte1, Data = 2B (hex), Read Byte1

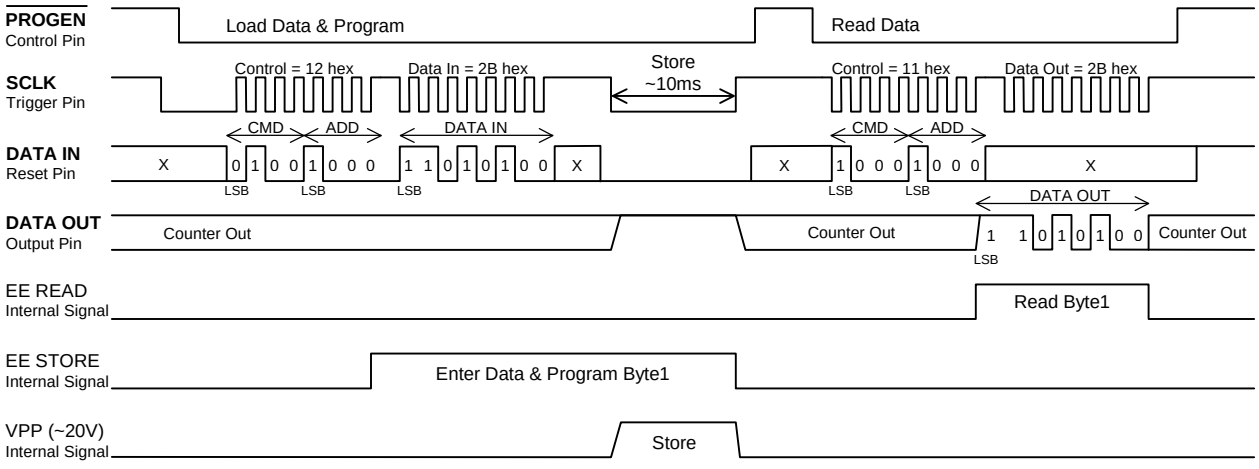

Figure 4

Serial Interface Timing Specifications

V_{DD} = 1.5V to 5.5V, Temperature = -40℃ to +85℃

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Clock Period	t_{CLKP}	50% duty cycle	500	200		ns
Serial Clock High Time	t_{CLKH}	Rising to falling edge	250	100		ns
Serial Clock Low Time	t_{CLKL}	Falling to rising edge	250	100		ns
Serial Clock Rise/Fall Times	t_R, t_F	20% to 80%, 80% to 20%			100	ns
Data In Setup Time	t_{DSU}	Data valid to rising clock edge	50	25		ns
Data In Hold Time	t_{DHD}	Falling clock edge to data invalid	50	25		ns
Mode Lead Time	t_{MLD}	Control pin low to first clock edge	1000	500		ns
Data Output Delay Time	t_{DOD}	Rising clock edge to Data Out valid		50	100	ns
EEPROM Store Time	t_{STR}	Clock low time (17th pulse)	25	10	100	millisec

Note 1: Typical values are for operation at 3V, 25°C

Note 2: Data Output Delay Time (t_{DOD}) measured with C_{LOAD} = 10pF and R_{LOAD} = 1MΩ.

Table 4

Serial Interface Timing Diagram

Read Mode

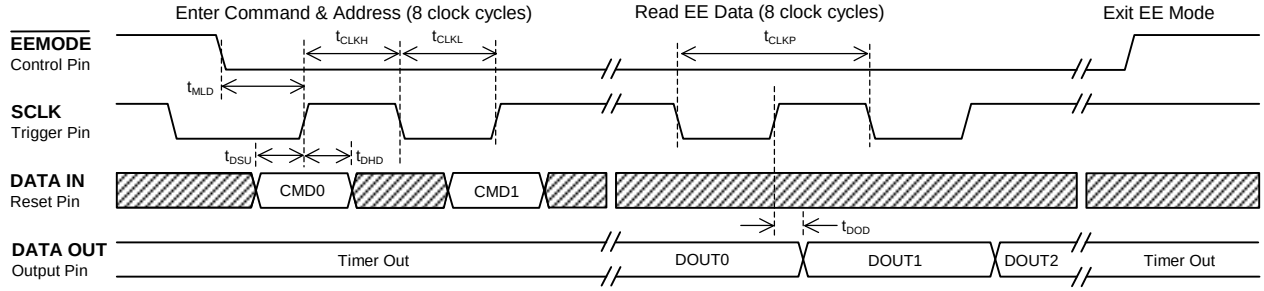

Figure 5

Program Mode

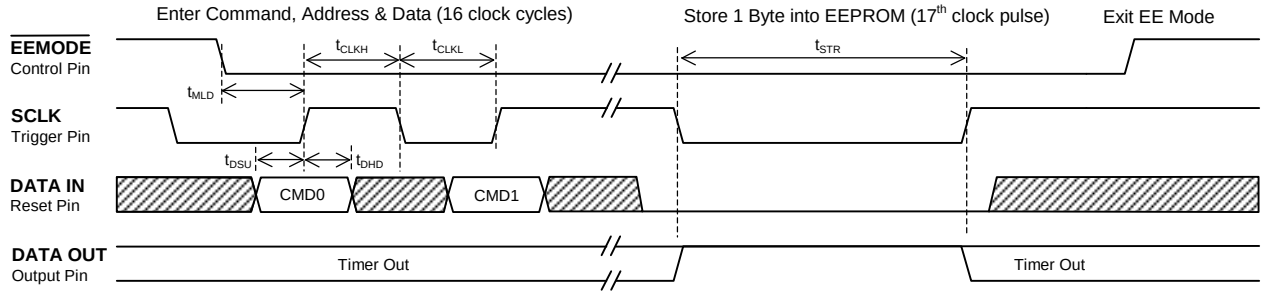

Figure 6

Serial Interface Examples

The CSS555's serial interface is very straightforward and requires minimal extra components to implement. It consists of three digital input signals that provide control, clock and data input functions and a single digital output that allows data to be read back from the device. The hardware needed to program the EEPROM depends on whether the IC is "loose" or has been installed in a system. Examples for both conditions are shown in Figures 7, 8 and 9.

Programming Before Installation

The circuit in Figure 7 shows a diagram for an interface schematic between an ATE (Automatic Test Equipment) and an uninstalled or "loose" IC. This example allows data to be written to and read from the internal EEPROM. No external components are required for this programming setup. (The timing components R_A, R_B and C have been omitted.)

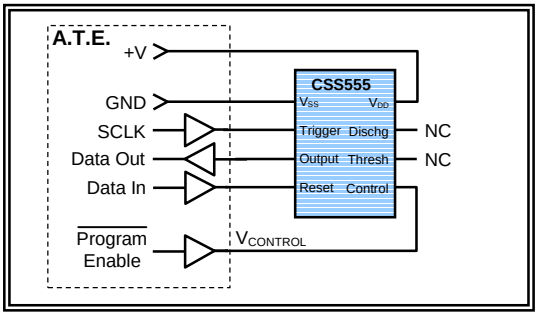

Figure 7
Program & Read EEPROM Only

If the timer function also needs to be tested, the circuit in Figure 8 shows an interface circuit that supports the Read, Write and Timer operating modes. The timing components R_A, R_B and C have been added. The output driver that provides the $V_{CONTROL}$ signal has been changed to a three-state output buffer. The normal timer mode is enabled when the $V_{CONTROL}$ buffer is disabled (OE=0). This allows the IC to set the voltage level at the CONTROL pin, which is about $\frac{2}{3}V_{DD}$. A timer cycle is started by pulsing SCLK (Trigger) low. (Reset/Data In must be held high.)

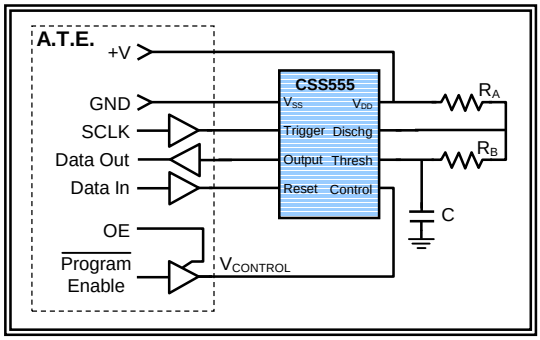

Figure 8
Program, Read and Timer Functions

Programming After Installation

If the CSS555 has been installed into a system, the changes required to implement the serial interface are still relatively minor. An example of one approach is shown in Figure 9. Test points TP1-TP4 have been added to provide access to the TRIGGER, RESET, CONTROL and OUTPUT pins. If three-state buffers are used to generate the test signals, the device can still be operated in the timer mode. In addition to the test port, resistors R_1 and R_2 have been added to allow the external ATE or "Programmer" to control the TRIGGER and RESET signals. Since these pins are high impedance CMOS inputs, the additional series resistance will not affect their operation or increase the operating current of the circuit. A value between 10KΩ to 100KΩ is suggested for R_1 and R_2.

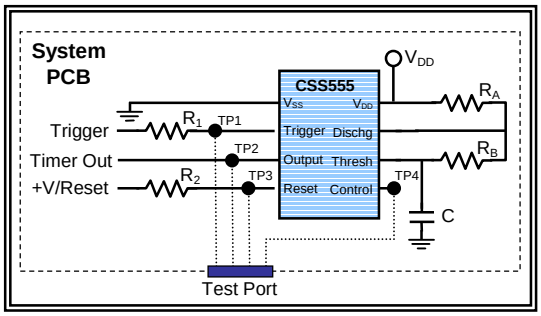

Figure 9
Program and Read "In the System"